SOLID-STATE IMAGING DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-078577; filed April 07, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a solid-state imaging device.

BACKGROUND

A solid-state imaging device includes a semiconductor substrate, and the semiconductor substrate includes a pixel area and a peripheral area. Pixels including photoelectric conversion elements are arranged in a matrix in the pixel area. Elements which operate the pixels and process signals output from the pixels are provided in the peripheral area. Generally, a solid-state imaging device converts an analog pixel signal output from a pixel into a digital pixel signal, and transfers the digital signal to a signal processing circuit. The solid-state imaging device performs reading of the analog pixel signal in each row of the pixels. The analog pixel signals which are output are supplied to comparators which are arranged in each column of the pixels to be compared to a reference voltage, the compared time is measured by counters, and thereby the analog pixel signal is converted into a digital pixel signal. At this time, if the counters which are arranged in a row direction simultaneously operate, current consumption increases and thereby a power supply voltage drops.

An example of related art includes JP-A-2011-166379.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic circuit diagram illustrating a part of a configuration of a solid-state imaging device according to a first embodiment.

FIG. 2 is a timing chart illustrating an operation of the solid-state imaging device according to the first embodiment.

FIG. 3 illustrates clock pulses which are supplied to the solid-state imaging device according to the first embodiment.

FIG. 4 is another timing chart illustrating the operation of the solid-state imaging device according to the first embodiment.

FIG. 5 is a schematic circuit diagram illustrating a part of a configuration of a solid-state imaging device according to a modification example of the first embodiment.

FIG. 6 is a schematic circuit diagram illustrating a part of a configuration of a solid-state imaging device according to a second embodiment.

DETAILED DESCRIPTION

[0004]Exemplary embodiments provide a solid-state imaging device which can reduce power supply voltage drop.

[0005]In general, according to one embodiment, a solid-state imaging device includes a first pixel having a first photoelectric conversion element; a second pixel having a second photoelectric conversion element; a first comparator which compares a pixel signal that is output from the first pixel to a reference voltage; a second comparator which compares a pixel signal that is output from the second pixel to a reference voltage; a first measuring instrument which is coupled to the first comparator and a frequency generator; and a second measuring instrument which is coupled to the second comparator and another frequency generator through a delay circuit.

[0007]A first embodiment will be hereinafter described with reference to the accompanying drawings. In each drawing, the same symbols or reference numerals will be attached to the same configuration elements, and detailed description thereof will be omitted.

First Embodiment

[0008]A solid-state imaging device according to a first embodiment will be described with reference to FIG. 1 to FIG. 4. FIG. 1 is a schematic circuit diagram illustrating a part of a configuration of a solid-state imaging device according to a first embodiment. FIG. 2 is a timing chart illustrating an operation of the solid-state imaging device according to the first embodiment. FIG. 3 illustrates clock pulses which are supplied to the solid-state imaging device according to the first embodiment. FIG. 4 is another timing chart illustrating the operation of the solid-state imaging device according to the first embodiment.

[0009]The solid-state imaging device according to the first embodiment includes a pixel area 2 in which pixels 1 including photoelectric conversion elements are arranged in a matrix, a vertical scanning circuit 3 which scans the pixels 1 in a vertical direction, analog digital converters (ADC) 4 of a column type which are arranged in each column of each pixel 1, a reference voltage supplying unit 9, a horizontal scanning circuit 11, a horizontal output line 14, and a timing generator 8.

[0010]The pixel area 2 includes the pixels 1 which are arranged in a matrix. In the first embodiment, among the pixels 1 in a first row of the pixel area 2, the pixel 1 in a first column is referred to as a first pixel 1a, and the pixel 1 of a second column adjacent to the first column is referred to as a second pixel 1b. The pixel 1 includes a photo diode serving as a photoelectric conversion element, and a plurality of transistors. The photo diode performs a photoelectric conversion of light which is incident, and accumulates electric charges corresponding to an amount of light.

[0011]The plurality of transistors include a transfer transistor which transfers the electric charges accumulated in the photo diode to a floating diffusion node, a reset transistor which resets the floating diffusion node to a predetermined voltage, an amplification transistor which outputs a potential corresponding to a voltage of the floating diffusion node, and a select transistor which outputs a signal that is transferred by the amplification transistor to vertical signal lines 13 in accordance with a select signal. Meanwhile, detailed description of the transistors will be omitted.

[0012]The first pixel 1a is coupled to a first vertical signal line 13a, and the second pixel 1b is coupled to a second vertical signal line 13b. Ends of the first vertical signal line 13a and the second vertical signal line 13b are coupled to the ADCs 4 of a column type which are arranged in each column of the pixels. By doing so, the analog pixel signal which is output from the first pixel 1a is input to the ADC 4 of a column type through the first vertical signal line 13a. The analog pixel signal which is output from the second pixel 1b is input to the ADC 4 of a column type through the second vertical signal line 13b. Here, the analog pixel signal is a reset potential which is output from the pixel 1 as the vertical scanning circuit 3 outputs a reset signal, and a pixel potential which corresponds to an amount of electric charges accumulated in the photo diode and is output from the pixel 1 as the vertical scanning circuit 3 outputs a transfer signal. An operation thereof will be described later.

[0013]The vertical scanning circuit 3 is coupled to the pixels 1 in the pixel area 2. The vertical scanning circuit 3 outputs a transfer signal to the transfer transistor included in the pixel 1, outputs a reset signal to the reset transistor, and outputs a select signal to the select transistor. As each signal is output to the pixel 1, the transistors included in the pixel 1 operate, and an analog pixel signal is output from the pixel 1.

[0014]The ADC 4 of a column type converts an analog pixel signal which is output from the pixel 1 into a digital pixel signal, and transfers the digital pixel signal to a storage device 7. The ADC 4 of a column type includes a comparator 5 and a counter 6 serving as a measuring instrument. The transferred digital pixel signals are sequentially read by a signal which is generated by the horizontal scanning circuit 11, and are output to a signal processing unit 12 through a horizontal output line 14.

[0015]The timing generator 8 serving as a frequency generator is coupled to the vertical scanning circuit 3, the counter 6, the reference voltage supplying unit 9, a delay circuit 10, and the horizontal scanning circuit 11. The timing generator 8 generates a clock signal which is a reference of an operation, a control signal, or the like, and supplies the clock signal to the vertical scanning circuit 3, the reference voltage supplying unit 9, the counter 6, and the horizontal scanning circuit 11.

[0016]One terminal of the reference voltage supplying unit 9 is coupled to the timing generator 8, and the other terminal of the reference voltage supplying unit 9 is coupled to the comparator 5. The reference voltage supplying unit 9 generates a reference voltage Vref on the basis of the clock signal which is supplied from the timing generator 8. The reference voltage Vref has, for example, a ramp waveform or the like in which a waveform of a voltage is changed in an inclined manner as illustrated in FIG. 2. The reference voltage supplying unit 9 supplies the reference voltage Vref to the comparator 5.

[0017]The comparator 5 compares an analog pixel signal which is output from the pixel 1 to the reference voltage Vref which is output from the reference voltage supplying unit 9.

[0018]The comparators 5 are arranged in each column of the pixels 1, and are configured by a first comparator 5a corresponding to the first pixel 1a, and a second comparator 5b corresponding to the second pixel 1b.

[0019]An input terminal of the first comparator 5a is coupled to the first vertical signal line 13a and the reference voltage supplying unit 9, and an output terminal of the first comparator 5a is coupled to a first counter 6a.

[0020] An input terminal of the second comparator 5b is coupled to the second vertical signal line 13b and the reference voltage supplying unit 9, and an output terminal of the second comparator 5b is coupled to a second counter 6b.

[0021]The counter 6 is configured by the first counter 6a which receives an output of the first comparator 5a, the second counter 6b which receives an output of the second comparator 5b, and the like. The first counter 6a receives a clock pulse CLK of the timing generator 8. The second counter 6b receives a delayed clock pulse DCLK of the timing generator 8 through the delay circuit 10. The first counter 6a measures time in which an analog pixel signal is compared to the reference voltage Vref in the first comparator 5a. The second counter 6b measures time in which an analog pixel signal is compared to the reference voltage Vref in the second comparator 5b, but the measurement is performed later than the first counter 6a.

[0022]The delay circuit 10 is configured by, for example, a circuit in which an even number of inverters is coupled in series. If an even number of inverters is coupled to each other, the delay circuit 10 outputs the same signal as an input signal from a final inverter, thereby delaying time from an input of a signal to an output of the signal. In the first embodiment, a phase shift between the clock pulse CLK which is input to the first counter 6a and the delayed clock pulse DCLK which is input to the second counter 6b may be, for example, within a range which is shifted by approximately a half pulse from the clock pulse CLK serving as a reference, as illustrated in FIG. 3. In the first embodiment, the delay circuit 10 including four inverters coupled to each other is described, but the number of the inverters can be changed in accordance with time to be delayed, if the number of the inverters is even.

[0023]The storage device 7 is divided into a first storage device 7a which is coupled to the first counter 6a, and a second storage device 7b which is coupled to the second counter 6b. The storage device 7 stores values which are measured by each counter included in the counter 6.

[0024]The horizontal scanning circuit 11 is configured by a register or the like (not illustrated). The digital pixel signals stored in the storage devices of the storage device 7 which are arranged in each column of the pixels are sequentially read by a signal which is generated by the horizontal scanning circuit 11, and are output to the signal processing unit 12 through the horizontal output line 14.

[0025]Subsequently, an operation of the solid-state imaging device according to the first embodiment will be described.

[0026]As illustrated in FIG. 4, the vertical scanning circuit 3 outputs a select signal, and the pixel 1 in a first row is selected ((c) in FIG. 4). In a state in which the select signal is output, the vertical scanning circuit 3 outputs a reset signal ((a) in FIG. 4). By doing so, reset potentials serving as reference potentials of the pixels 1 are output from the first pixel 1a in the first row and the second pixel 1b in the second row. The reset potential which is output from the first pixel 1a is input to the first comparator 5a through the first vertical signal line 13a. In addition, the reset potential which is output from the second pixel 1b is input to the second comparator 5b through the second vertical signal line 13b.

[0027]Subsequently, the vertical scanning circuit 3 outputs a transfer signal ((b) in FIG. 4). By doing so, pixel potentials corresponding to the electric charges accumulated in the photo diode of the pixel 1 are output from the first pixel 1a in the first row and the second pixel 1b in the second row. The pixel potential which is output from the first pixel 1a is input to the first comparator 5a through the first vertical signal line 13a. In addition, the pixel potential which is output from the second pixel 1b is input to the second comparator 5b through the second vertical signal line 13b.

[0028]The reference voltage supplying unit 9 supplies the first comparator 5a and the second comparator 5b with the reference voltage Vref of a ramp type in which a voltage value is changed with the passage of time ((h) in FIG. 4). The first comparator 5a and the second comparator 5b perform a comparison operation of the reset potentials which are output from, for example, the pixels in the first and second rows and the reference voltage Vref, and a comparison operation of the pixel potentials and the reference voltage Vref ((g) and (h) in FIG. 4).

[0029]An operation in which the reset potential is input to the first comparator 5a in the first row will be first described.

[0030]After the reset potential which is input to the first comparator 5a is stabilized, the reference voltage supplying unit 9 supplies the reference voltage Vref to the first comparator 5a ((g) and (h) in FIG. 4). The timing generator 8 supplies the clock pulse CLK to the first counter 6a at the same time when the reference voltage Vref is supplied to the first comparator 5a (T1 of (i) in FIG. 4). As the first counter 6a supplies the clock pulse CLK, the first counter 6a counts comparison time of the reset potential and the reference voltage Vref which are compared by the first comparator 5a (T1 of (k) in FIG. 4). When the reference voltage Vref and the reset potential coincide with each other, the counter stops (T3 of (k) in FIG. 4).

[0031]Subsequently, an operation in which the pixel potential is input to the first comparator 5a in the first row will be described.

[0032]After the pixel potential which is input to the first comparator 5a is stabilized, the reference voltage supplying unit 9 supplies the reference voltage Vref to the first comparator 5a ((g) and (h) in FIG. 4). The timing generator 8 supplies the clock pulse CLK to the first counter 6a at the same time when the reference voltage Vref is supplied to the first comparator 5a (T4 of (i) in FIG. 4). As the first counter 6a supplies the clock pulse CLK, the first counter 6a counts comparison time of the pixel potential and the reference voltage Vref which are compared by the first comparator 5a ((k) in FIG. 4). When the reference voltage Vref and the pixel potential coincide with each other, the counter stops (T6 of (k) in FIG. 4). The first counter 6a performs subtraction processing of the number of the clock pulses included in a period in which second counting is performed from start to stop, and the number of the clock pulses included in a period in which first counting is performed from start to stop. As the subtraction processing is performed in this way, a reset component potential which includes noise of the pixel 1 is removed, and thereby it is possible to read signal components corresponding to the electric charges accumulated in the photo diode of the pixel 1. After the subtraction processing, the first counter 6a transfers the number of clock pulses to the storage device 7. The number of clock pulses which are stored in the storage device 7 is read to the signal processing unit 12 as a value of the digital pixel signal which is read from the pixel 1.

[0033]Subsequently, an operation in which the reset potential is input to the second comparator 5b in the second row will be described.

[0034]The reference voltage supplying unit 9 supplies the reference voltage Vref to the second comparator 5b ((h) in FIG. 4). The delayed clock pulse DCLK which is obtained by converting the clock pulse CLK through inverters is supplied to the second counter 6b at the same time when the reference voltage Vref is supplied to the second comparator 5b ((j) in FIG. 4). As the delayed clock pulse DCLK is supplied to the second counter 6b, the second counter 6b counts comparison time of the reset potential and the reference voltage Vref which are compared by the second comparator 5b (T2 of (l) in FIG. 4). Start time of the comparison of the reset potential and the reference voltage Vref in the second counter 6b is delayed by an amount of delay of the phase of the pulse, compared to the start time of comparison in the first counter 6a (T2 of FIG. 4). When the reference voltage Vref and the reset potential coincide with each other, the counter 6 stops (T3 of (l) in FIG. 4).

[0035] Subsequently, an operation in which the pixel potential is input to the second comparator 5b in the second row will be described.

[0036]After the pixel potential which is input to the second comparator 5b is stabilized, the reference voltage supplying unit 9 supplies the reference voltage Vref to the second comparator 5b ((h) in FIG. 4). The delayed clock pulse DCLK is supplied to the second counter 6b at the same time when the reference voltage Vref is supplied to the second comparator 5b ((j) in FIG. 4). As the delayed clock pulse DCLK is supplied to the second counter 6b,the second counter 6b counts comparison time of the pixel potential and the reference voltage Vref which are compared by the second comparator 5b (T5 of (l) in FIG. 4). Start time of the comparison of the pixel potential and the reference voltage Vref in the second counter 6b is delayed more than the start time of comparison in the first counter 6a (T5 of FIG. 4). When the reference voltage Vref and the pixel potential coincide with each other, the counter stops (T6 of (l) in FIG. 4). The second counter 6b performs subtraction processing at the same time as the first counter 6a. After the subtraction processing, the subtracted value is transferred to the storage device 7 to be stored.

[0037]Meanwhile, the aforementioned operations of the first comparator 5a and the second comparator 5b are simultaneously performed for each row in the pixel area 2. After the operation for the first row in the pixel area 2 is completed, the horizontal scanning circuit 11 reads the digital pixel signals stored in the storage device 7 in each column to the horizontal output line 14. The digital pixel signals which are read to the horizontal output line 14 are supplied to the signal processing unit 12.

[0038]In the first embodiment, an inverter that is the delay circuit 10 is provided between the timing generator 8 and the second counter 6b. Accordingly, the second counter 6b operates later than the first counter 6a. As the first counter 6a and the second counter 6b simultaneously operate, current consumption can be reduced, and thereby it is possible to prevent the power supply voltage from dropping. For this reason, elements which operate using the same power supply can reduce noise or the like which is generated by the power supply voltage drop.

[0039]Meanwhile, in the first embodiment, the first column and the second column of the first row in the pixel area 2 are described, but the other rows and columns are the same. That is, the clock pulse CLK is directly supplied from the timing generator 8 to the counter in a odd-numbered row of a third column or the like, and the delayed clock pulse DCLK which is output through an inverter is supplied to the counter in an even-numbered column of a fourth row or the like. In this way, the counters 6 in the first column and the third column perform counting at the same timing as each other, and the counters 6 in the second column and the fourth column perform counting at the same timing as each other. In this way, as the counters 6 adjacent to each other shift counting, it is possible to prevent a voltage from dropping due to a simultaneous operation of the counters 6.

[0040]In the first embodiment, an example in which the clock pulse CLK is supplied to the first column in the pixel area and the delayed clock pulse DCLK is supplied to the second column is described, but the delayed clock pulse DCLK may be supplied to the first column, and the clock pulse CLK may be supplied to the second column.

[0041]Subsequently, a modification example of the solid-state imaging device according to the first embodiment will be described with reference to FIG. 5. FIG. 5 is a schematic circuit diagram illustrating a part of a configuration of a solid-state imaging device according to a modification example of the first embodiment. The modification example is different from the first embodiment in that a first switching element 20 is provided between the second vertical signal line 13b and the second comparator 5b, and a second switching element 21 is provided between the timing generator 8 and an inverter serving as the delay circuit 10.

[0042]The solid-state imaging device according to the modification example has a binning structure. Binning means that a plurality of pixels 1 operates as one pixel. In the binning structure, when the first pixel 1a and the second pixel 1b are regarded as a pixel group 50, for example, the first switching element 20 is provided between the second vertical signal line 13b coupled to the second pixel 1b and the second comparator 5b, as illustrated in FIG. 5. In addition, the second switching element 21 is provided between the timing generator 8 and an inverter. When the first switching element 20 is turned on, the second pixel 1b is coupled to the second comparator 5b, and thereby the analog pixel signals which are output from each column of the pixels 1 are input to the comparator 5. When the first switching element 20 is turned off, the analog pixel signals which are output from the first pixel 1a and the second pixel 1b are input to the first comparator 5a. In this structure, only the first counter 6a may operate, and thus it is possible to prevent the power supply voltage from dropping due to an increase of current consumption. In addition, when the first switching element 20 is turned off, the analog pixel signal is not input to the second comparator 5b, and thus it is not necessary to operate the second counter 6b corresponding to the second comparator 5b. At this time, the second switching element 21 is turned off, and thus the inverter may not operate. In this way, the first switching element 20 and the second switching element 21 are provided, and thereby current consumption can be suppressed from increasing, even in the solid-state imaging device having the binning structure. Thus, it is possible to prevent the power supply voltage from dropping.

Second Embodiment

[0043]A solid-state imaging device according to a second embodiment will be described using FIG. 6. FIG. 6 is a schematic circuit diagram illustrating a part of a configuration of a solid-state imaging device according to a second embodiment.

[0044]The solid-state imaging device according to the second embodiment is different from the first embodiment in that two inverters having a different number of inverters from each other are coupled to a selector 17. One of the delayed clock pulses DCLK which are output from the two inverters is supplied to the counter 6 by a select control signal which is input to the selector 17. The solid-state imaging device according to the second embodiment has the same structure as the solid-state imaging device according to the first embodiment except for the above-described point. Thus, the same symbols or reference numerals are attached to the same portions, and detailed description thereof will be omitted.

[0045]A structure of the solid-state imaging device according to the second embodiment will be described.

[0046]The counter 6 is configured by a first counter 6a which receives an output of the first comparator 5a, and a second counter 6b which receives an output of the second comparator 5b. The first counter 6a receives the clock pulse CLK of the timing generator 8. The second counter 6b receives the delayed clock pulse DCLK of the timing generator 8 through the delay circuit 10. The first counter 6a measures the time which is taken by comparing the analog pixel signal to the reference voltage Vref in the first comparator 5a. The second counter 6b measures the time which is taken by comparing the analog pixel signal to the reference voltage Vref in the second comparator 5b, but the measurement is performed later than the first counter 6a.

[0047]The delay circuit 10 including two inverters having a different number of inverters from each other is coupled to the selector 17. In the second embodiment, an example in which two inverters are coupled to the selector 17 is described, but a plurality of inverters may be coupled to the selector 17.

[0048]One terminal of the selector 17 is coupled to two inverters, and the other terminal of the selector 17 is coupled to four inverters. If the number of inverters which are coupled is even and different from each other, the number is not limited. By doing so, the two clock pulses input to the inverters can be converted into two delayed clock pulses DCLK whose phases are shifted with respect to the clock pulse CLK serving as a reference.

[0049]The selector 17 is coupled to a select control signal line sel. The select control signal is supplied to the selector 17 through the select control signal line sel. The select control signal selects an optimum delayed clock pulse DCLK among the delayed clock pulses DCLK which are output from the two inverters. Among the two delayed clock pulses DCLK, one pulse which is selected by the select control signal is supplied to the second counter 6b.

[0050]Accordingly, an optimum value of a delayed time is selected, and the selected value can be supplied to the second counter 6b. Since the counted times which are measured by the first counter 6a and the second counter 6b are different from each other, it is possible to prevent the power supply voltage from dropping. For this reason, elements which operate by using the same power supply can reduce noise or the like which is generated by dropping of the power supply voltage.

[0051]In the second embodiment, the selector 17 is provided between the timing generator 8 and the second counter 6b, and two inverters having a different number of inverters from each other are coupled to the selector 17. Since an optimum value of the delayed time is selected and the optimum value is supplied to the second counter 6b, the second counter 6b can operate later than the first counter 6a. For this reason, the first counter 6a and the second counter 6b simultaneously operate, and thus it is possible to prevent the power supply voltage from dropping due to an increase of the current consumption.

[0052]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A solid-state imaging device comprising:

a first pixel having a first photoelectric conversion element;

a second pixel having a second photoelectric conversion element;

a first comparator which compares a pixel signal that is output from the first pixel to a reference voltage;

a second comparator which compares a pixel signal that is output from the second pixel to a reference voltage;

a first measuring instrument which is coupled to the first comparator and a frequency generator; and

a second measuring instrument which is coupled to the second comparator and another frequency generator through a delay circuit.

2. The device according to Claim 1, wherein the delay circuit is configured by even-numbered inverters which are coupled to each other.

3. The device according to Claim 1,

wherein the delay circuit includes a selector which can select a first inverter having even-numbered inverters that are coupled to each other, and a second inverter having a number of inverter different from the first inverter, and

wherein one of delayed clock pulses which are converted by the first inverter and the second inverter using a select control signal is supplied to the second comparator.

4. The device according to Claim 1, wherein the first measuring instrument is a first counter, and the second measuring instrument is a second counter.

5. The device according to Claim 1, wherein the first pixel and the second pixel respectively include a plurality of transistors.

6. The device according to Claim 5, wherein the plurality of transistors include a transfer transistor and a reset transistor.

7. The device according to Claim 6, wherein the plurality of transistors further include a select transistor.

8. The device according to Claim 1, wherein the first pixel and the second pixel are adjacent to each other in a row direction.

ABSTRACT

A solid-state imaging device according to an embodiment includes a first pixel having a first photoelectric conversion element; a second pixel having a second photoelectric conversion element; a first comparator which compares a pixel signal that is output from the first pixel to a reference voltage; a second comparator which compares a pixel signal that is output from the second pixel to a reference voltage; a first measuring instrument which is coupled to the first comparator and a frequency generator; and a second measuring instrument which is coupled to the second comparator and another frequency generator through a delay circuit.

Drawings

FIG. 2

ANALOG PIXEL SIGNAL

RESET POTENTIAL

PIXEL SIGNAL

REFERENCE VOLTAGE Vref

FIG. 3

CLOCK PULSE CLK

DELAYED CLOCK PULSE DCLK

FIG. 4

(a) RESET SIGNAL (FIRST ROW)

(b) TRANSFER SIGNAL (FIRST ROW)

(c) SELECT SIGNAL (FIRST ROW)

(d) RESET SIGNAL (SECOND ROW)

(e) TRANSFER SIGNAL (SECOND ROW)

(f) SELECT SIGNAL (SECOND ROW)

(g) ANALOG PIXEL SIGNAL

(h) REFERENCE VOLTAGE Vref

(i) CLOCK PULSE CLK (FIRST COLUMN)

(j) DELAYED CLOCK PULSE DCLK (SECOND COLUMN)

(k) COUNTER (FIRST COLUMN)

(l) COUNTER (SECOND COLUMN)

RESET POTENTIAL

PIXEL POTENTIAL

RESET POTENTIAL

PIXEL POTENTIAL